sames

SA2532KA/B

SINGLE CHIP TELEPHONE FOR INDIA

Key Features

- Speech Circuit, LD/MF Dialler and Tone Ringer on one 28 pin CMOS chip
- Low Noise
- 31 digit Last Number Redial
- Line Loss Compensation selectable by pin option
- 2 Timed Break Recall keys
- Moving Cursor protocol with comparison
- On chip MF filter (CEPT CS 203 compatible)
- Pause key for auto pause or wait function
- Power down mode
- Ring frequency discrimination
- Selectable Loop-Disconnect or DTMF dialling modes
- Real or complex impedance programmable
- Soft Clipping to avoid harsh distortion
- Uses inexpensive 3.58MHz ceramic resonator
- Operating range from 13 to 100 mA
- 3 Tone melody generator

General Description

The SA2532K is a CMOS integrated circuit that contains all the functions needed to form a high performance electronic telephone.

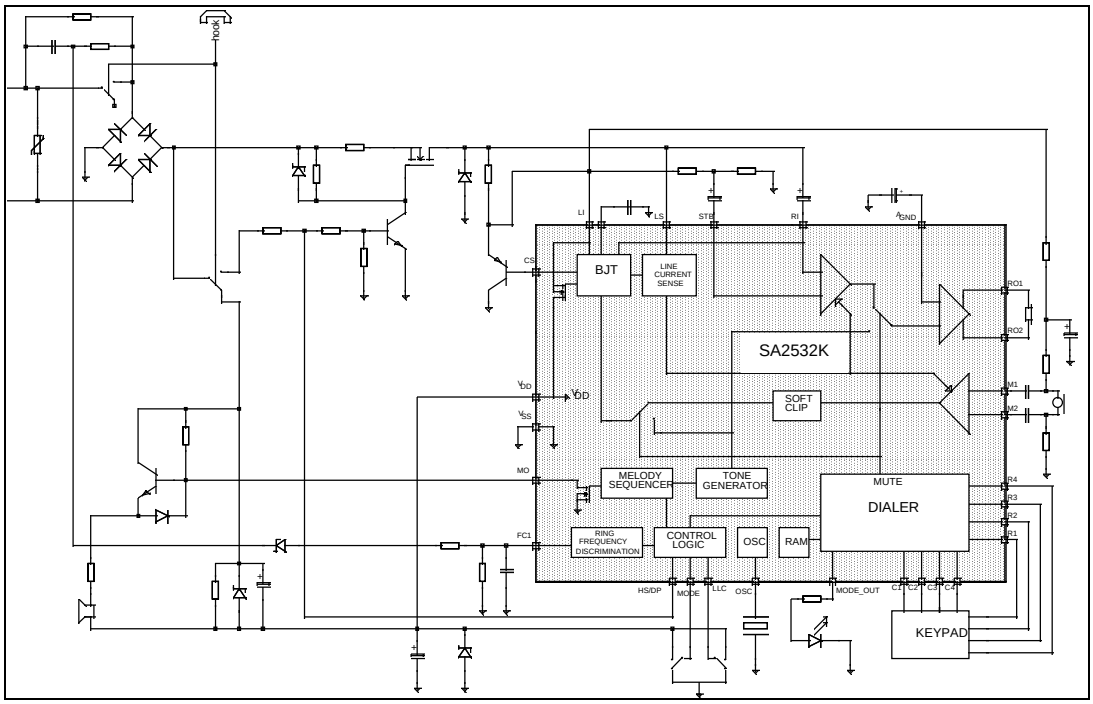
The device incorporates LD/MF repertory dialling, melody generation, ring frequency discrimination and a high quality speech circuit.

Soft switch into temporary MF mode using * when LD mode is selected .Timed Break Recall will be available in both LD and MF dialling modes.

A 31 digit Last Number Redial (LNR) memory, with moving cursor protocol, activated by single key depression.

Line Loss Compensation whereby send and receive gains are adjusted (by 6dB) over the ranges selected by the LLC pin.

Block Diagram



Package
Available in 28 pin DIP.

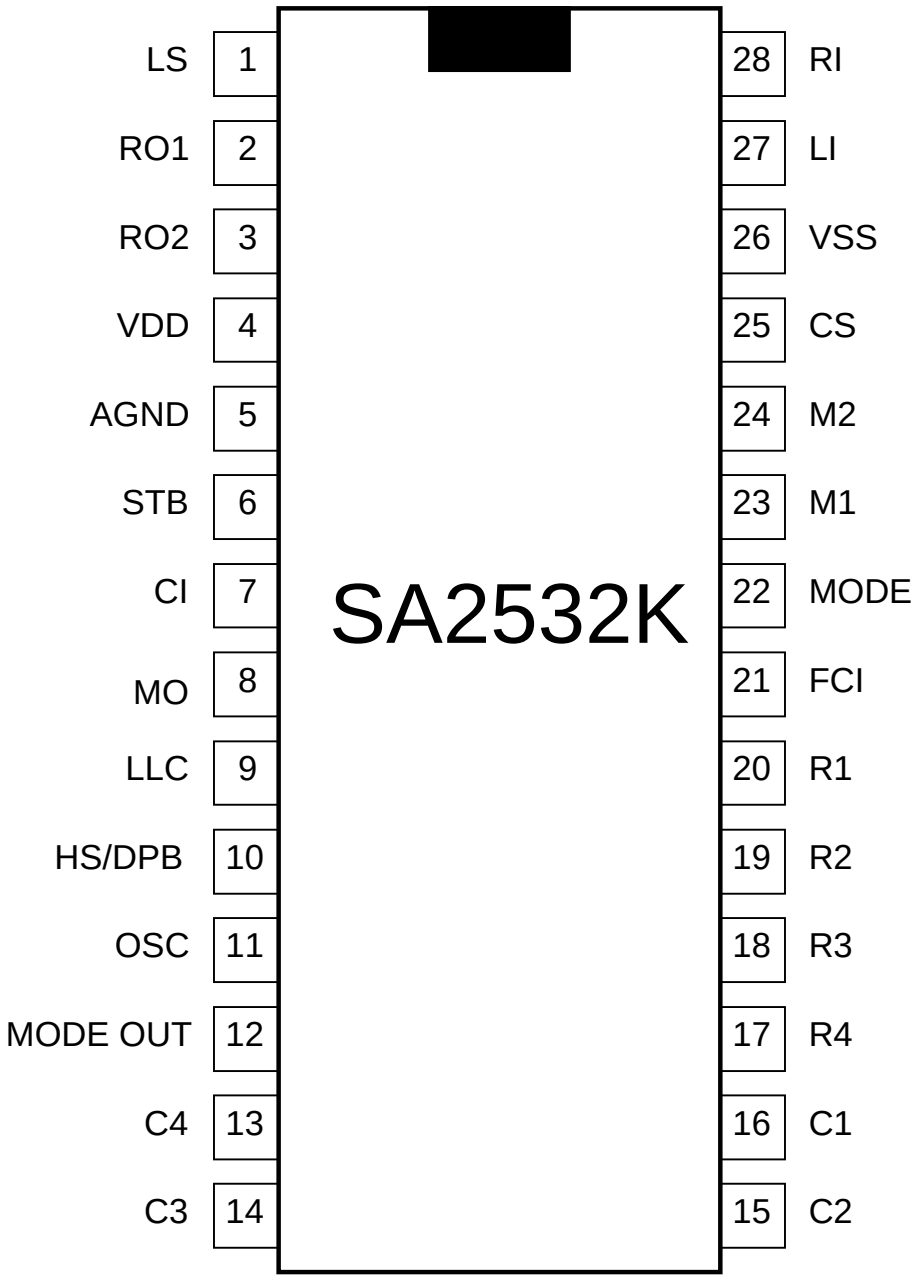


Figure 1

Pin Description

Pin #	Symbol	Function
23 24	M1 M2	**Microphone Inputs** Differential inputs for the microphone (electret).
2 3	RO1 RO2	**Receiver Outputs** These are the outputs for driving a dynamic ear piece with an impedance of 100 to 300Ohms
5	A_{GND}	**Analog Ground** This is the analog ground for the amplifiers.
28	RI	**Receive Input** This is the input for the receive signal.
6	STB	**Side Tone Balance Input** This is the input for side tone cancellation.
1	LS	**Line Current Sense Input** This is the input for sensing the line current.
27	LI	**Line Input** This input is used for power extraction and line current sensing.
25	CS	**Current Shunt Control Output** This N-channel open drain output controls the external high power shunt transistor for the modulation of the line voltage and for shorting the line during make period of pulse dialling.
4	V_{DD}	**Positive Voltage Supply** This is the supply pin for the circuit.
26	V_{SS}	**Negative Power Supply**
8	MO	**Melody Output** Pulse Density Modulated output of the melody generator for tone ringer. At high impedance when not active.
21	FCI	**Frequency Comparator Input** This is a Schmitt trigger input for ring frequency discrimination. Disabled during off-hook.
10	HS/DPB	**Hook Switch Input and Dial Pulse Output** This is an I/O that is pulled high by the hook switch when off- hook. An open drain pulls it low during break periods of pulse dialling and flash.
11	OSC	**Oscillator Input** Oscillator pin for Xtal or ceramic resonator (3.58 Mhz). Recommended : Murata CSA 3.58MG312AM
12	MODE OUT	**Mode Output.** An Output pin designed to drive a low power LED. Active whenever MF dialling mode is selected.
9	LLC	**Line Loss Compensation.** Select pin for the line loss compensation: Open None Low 20-50mA High 45-75mA

Pin Description Cont'd

Pin #	Symbol	Function
22	MODE	**Signalling Mode Select Input** Mode pin Function High LD default mode, make/break = 33/66 ms Open MF only Low LD default mode, make/break = 40/60 ms
20 19 18 17	R1 R2 R3 R4	**Keyboard Rows**
16 15 14 13	C1 C2 C3 C4	**Keyboard Columns**
7	CI	**Complex Impedance Input** Input pin for the capacitor in the complex impedance

Keyboard Connections

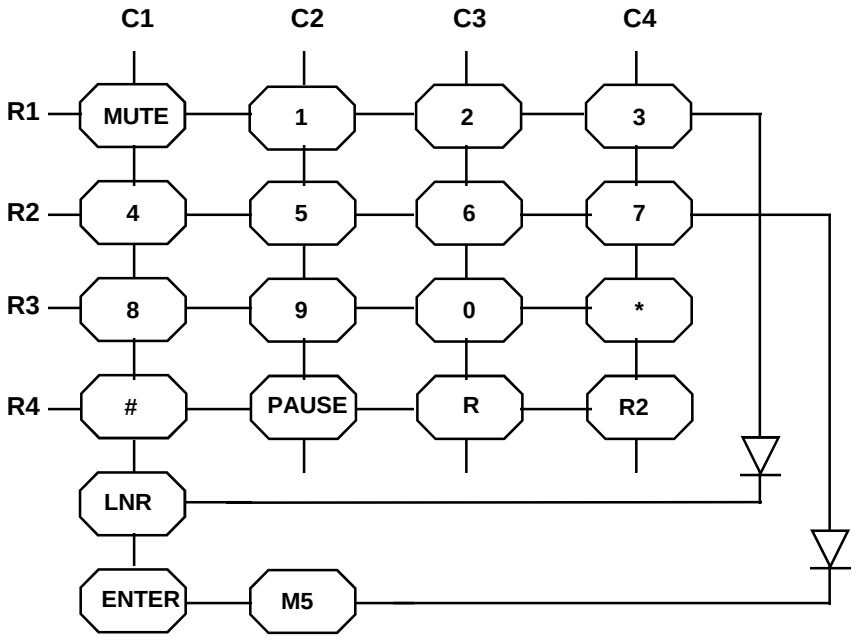


Figure 2

Power On Reset

The on chip power on reset circuit monitors the supply voltage (V_{DD}). When V_{DD} rises above approx. 1.2V, a power on reset occurs to assure correct start-up and the LNR register is cleared.

DC Conditions

The normal operating range is from 15mA to 100 mA. Operating range with reduced performance is from 5mA to 15mA. In the operating range all functions are operational. In the line hold range from 0 to 5 mA the device is in a power down mode and the voltage at LI is reduced to maximum 3.5V. The dc characteristic (excluding diode bridge and Pulsing transistors) is determined by the voltage at LI and the resistor R1 as follows:

$$VLS = VLI + I_{Line}.R1$$

The voltage at LI is 4.5V.

During pulse dialling the speech circuit and other parts of the device not required are in a power down mode to save current. The CS pin is pulled to V_{SS} in order to turn the external shunt transistor on to keep a low voltage drop at the LS pin during make periods.

AC Impedance

The Characteristic or Output impedance of the SA2532K is set within the IC and adjusted to 600 Ohms. A capacitor may be added to the circuit at pin CI to add a reactive element and make the output impedance complex.

Oscillator

All the Timing Functions of the SA2532K are based on a Clock Frequency of 3.58MHz. A ceramic resonator of this frequency should be connected to the OSC pin. In practice minor deviations from the nominal frequency may occur due to the characteristics of the frequency reference device used and so it is recommended that care is taken in the selection of components. Typically a small value capacitor ($\leq$ 47pF) may be required to be connected in parallel with the Frequency Reference to ensure start-up and/or operation at the nominal frequency.

Speech Circuit

The speech circuit consists of a transmit and a receive path with soft clip, mute, line loss compensation and side tone cancellation.

Transmit

The gain of the transmit path is 35 dB for M1/M2 to LS (see test circuit in Figure 5). The microphone input is differential with an input impedance of 25 kOhms. The soft clip circuit limits the output voltage at LI to $2.0V_{PEAK}$. The attack time is 30us/6dB and the decay time is 20 ms/6 dB. When mute is active, during dialling or after pressing the MUTE key, the gain is reduced by > 60 dB.

Receive

The receive input is the differential signal of RI and STB. The gain of the receive path is 2 dB (see test circuit in Figure 5) with differential outputs, RO1/RO2 . When mute is active during dialling the gain is reduced by > 60dB. During DTMF dialling a MF comfort tone is applied to the receiver. The comfort tone is the DTMF signal with a level that is -30dB relative to the line signal.

Side Tone

Side Tone is controlled along with Return Loss by a Double Balance Bridge as shown in Figure 3. Good sidetone cancellation is achieved by using the following equation:

$$\frac{Z_{bal}}{Z_{line}} = \frac{R5}{R1}$$

The side tone cancellation signal is applied to the STB input.

Line Loss Compensation

The line loss compensation is a pin selectable option. When it is activated, the gains of the transmit and receive amplifiers are changed by 6dB in accord with the DC conditions as measured at Pins LI and LS. When the LLC pin is low the adjustment in gain occurs over the range I_{LINE} = 20 to 50mA. When the LLC pin is high the gain range is I_{LINE} = 45 to 75mA.. Note that these values apply for R1 = R30 Ω. When LLC pin is open then the amplifier gains remain fixed regardless of the line current (see figure 6 and figure 7).

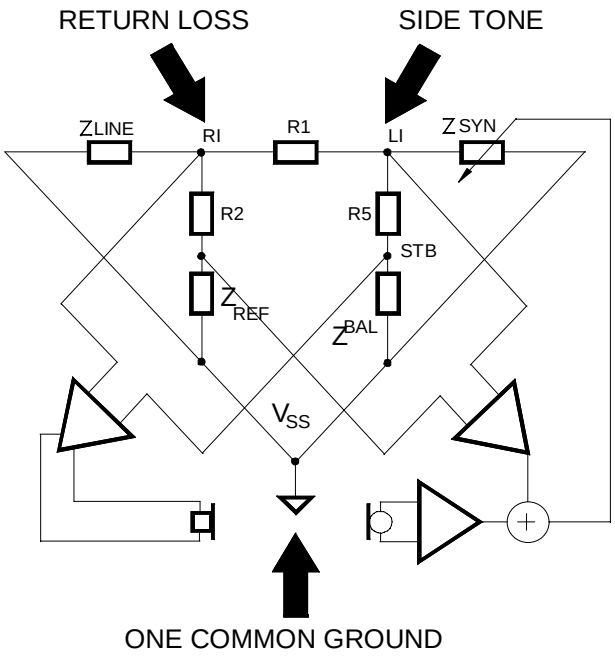


Figure 3

Double balanced bridge (return loss and side tone) with one common ground

Dialling Functions

Valid Keys

The keypad of the SA2532K comprises a maximum of 19 keys. A Bi-polar scan technique is used so that the 19 keys are scanned in a partial 4 x 6 matrix using only 8 pins and 2 diode. The key scanning is enabled when HS/DPN is pulled high and V_{DD} is above V_{REF}. A valid key is detected when one and only one contact closure is detected between a Row and Column Pin. Key contacts are debounced to avoid incorrect detection. It is also possible to connect a controller to the rows and columns.

Dial Mode Selection

The default mode (LD or MF) can be selected by the Mode pin. When default LD mode is selected, a temporary change to MF can be invoked by pressing the * key. Once in MF mode the MODE OUT pin becomes active. The circuit will revert to LD by pressing either one of the Recall keys or by next on-hook.

When MF mode is selected by the mode pin, the circuit can not be changed temporary to LD but will remain in MF. In LD mode the speech circuit will be muted for the duration of the IDP.

Last Number Redial

LNR is a facility that allows re-signalling of the last manually dialled number without keying in all the digits again. The LNR is repeatable. A manually entered number is automatically stored in the LNR RAM. The capacity of the LNR RAM is 31 digits. If a number greater than 31 digits is entered, the LNR facility will be inhibited (Until new entries < 32 digits) and further entries will be buffered in a First In First Out Memory (FIFO). Post dialled digits, i.e. digits manually entered after LNR has been invoked, are not stored in RAM but buffered in FIFO.

Pauses can be inserted by pressing the PAUSE key. Each pause is 2 seconds when inserted within the first 5 digits otherwise a wait function will halt dialling until PAUSE or LNR key is depressed.

Recall Function

A Recall activation will invoke a Flash (Timed Loop Break).

If Recall is the first entry in a digit string, it will be stored in LNR RAM when digit(s) are entered after the Recall.

If the recall key is depressed after a digit string has been entered or dialled out, the recall will not be stored but buffered in the FIFO together with subsequently entered digits.

If pressing the recall key is not followed by digit entries, the LNR RAM remains intact. After a recall a 274ms second pause will automatically be executed.

Both Recall keys will be functional in both MF and LD dialling modes.

Memory Keys

The single memory (M5) can be used to directly access a stored number of not more than 21 digits. During programming multiple pauses can be inserted by pressing the PAUSE or LNR key. Each pause is 3 seconds long when inserted within the first 5 digits otherwise a wait function (infinite pause) will be executed until the PAUSE or LNR key is depressed

Mute Function

The MUTE key is enabled in speech mode only. Depressing the MUTE key mutes the microphone amplifier. Repressing the MUTE key deactivates the mute (toggle function). Any key entry overwrites a mute activated by the MUTE key and mute will be deactivated.

When privacy mute is activated a reminder tone is applied to the ear piece every 274ms.

Moving Cursor Procedure

To accommodate easy and uncomplicated redialling (LNR) behind a PABX, a sliding cursor protocol is implemented. If new entries match the previous RAM contents, pressing the LNR key will dial out the remaining digits. If there is an error in matching, the LNR will be inhibited until next on-hook, and the RAM will contain the new number. In the case of mixed mode LNR operation the redialling in the SA2532KA is limited to the LD digits so as to prevent unauthorised access to banking passwords etc. The SA2532KB will dial out all digits (i.e. both the pulse and the DTMF digits) during mixed mode re-dialling.

DTMF Tones

The DTMF generator provides 7 frequencies, namely:

Low group	
Digit 1-2-3	697Hz
Digit 4-5-6	770Hz
Digit 7-8-9	852Hz
Digit *-0-#	941Hz

High group	
Digit 1-4-7-*	1209Hz
Digit 2-5-8-0	1336 Hz
Digit 3-6-9-#	1477Hz

The MF output levels are -6/-8 dBm and the preemphasis is 2.6dB.

Tone Ringer

The Tone Ringer of the SA2532K incorporates a Discriminator Circuit and a three tone Melody Generator.

When a Valid Ring Signal is detected the Melody generator is activated and creates a ringing signal comprising 3 frequencies F1 (1065Hz), F2 (1420Hz) and F3 (1734Hz).

These frequencies are repeated in a sequence of 6 time slots constructed by the frequencies

F1 F2 F3 F1 F2 F3

This sequence is repeated 7 times per second.

Ring Frequency Discrimination

The Ring Frequency Discriminator assures that signals with a frequency between 13 Hz to 70 Hz are regarded as valid ring signals. When a valid ring signal is detected, the melody generator is activated and remains active as long as the ring signal is present. Once the melody generator has been started, the ring signal is continuously monitored and the melody generator is instantly turned on or off according to the momentary presence of a valid or invalid ring signal respectively (until next POR of off-hook).

Typical Application

Only the components necessary for presenting the complete functions of the SA2532K are included.

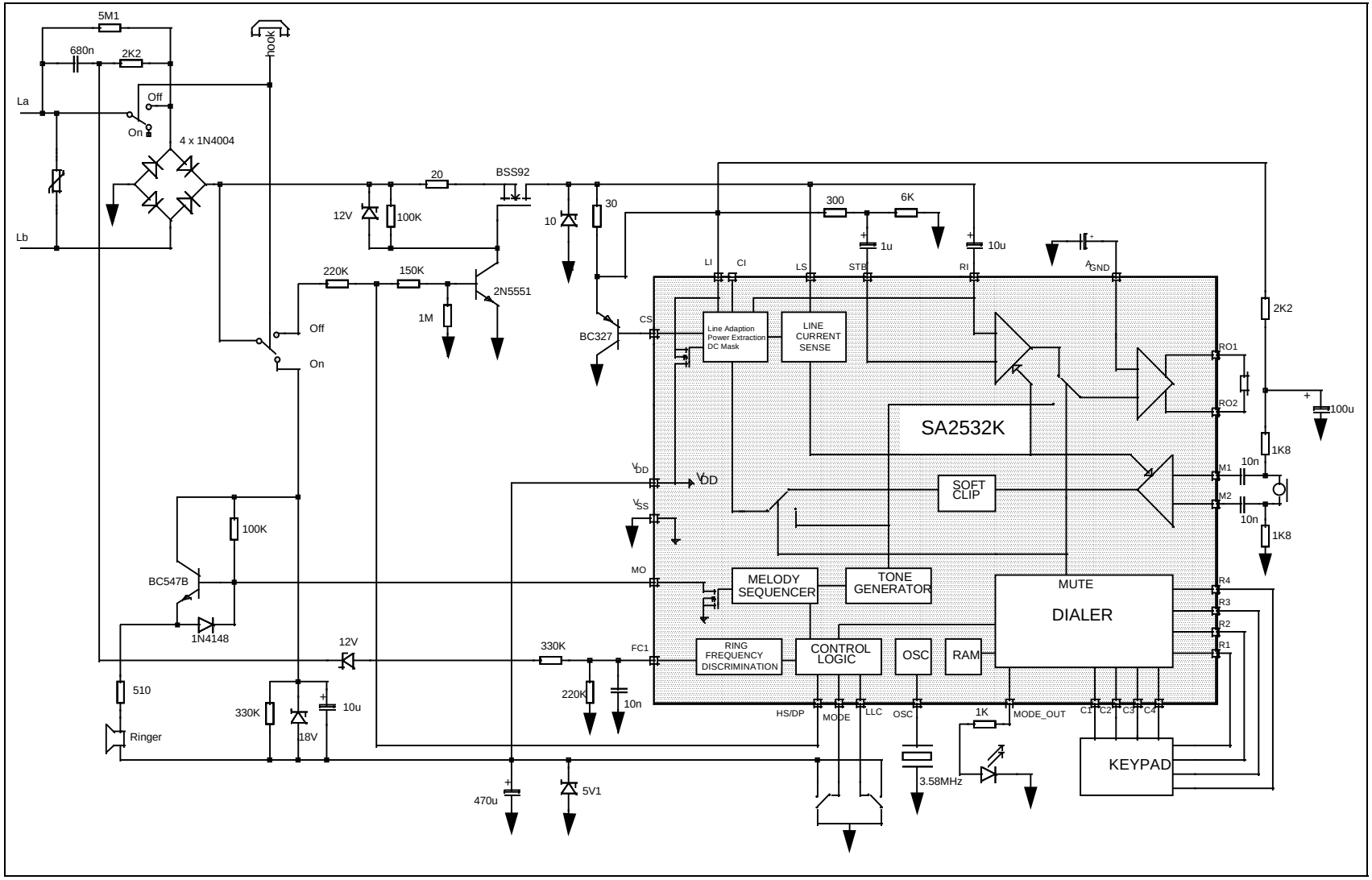
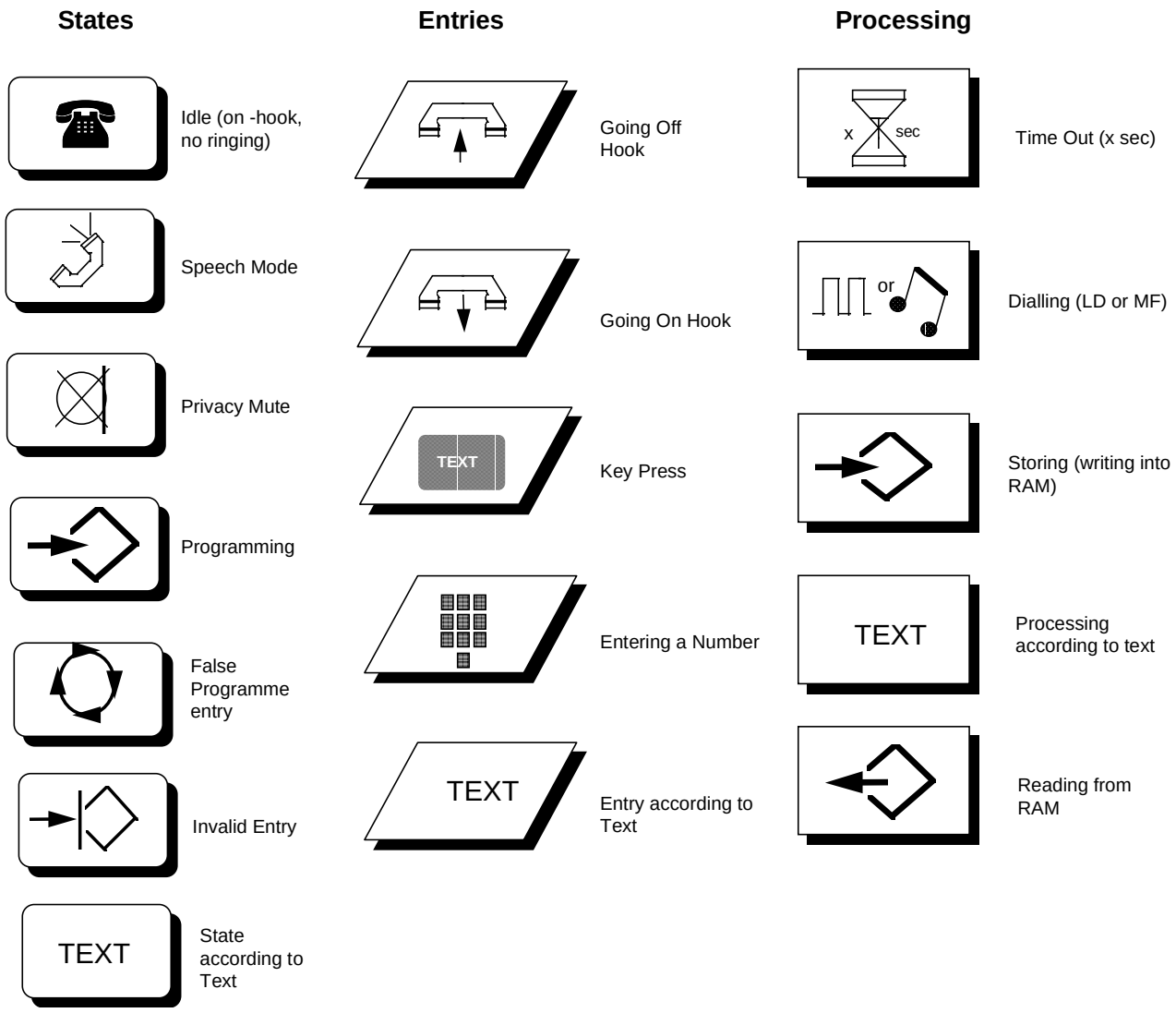


Figure 4

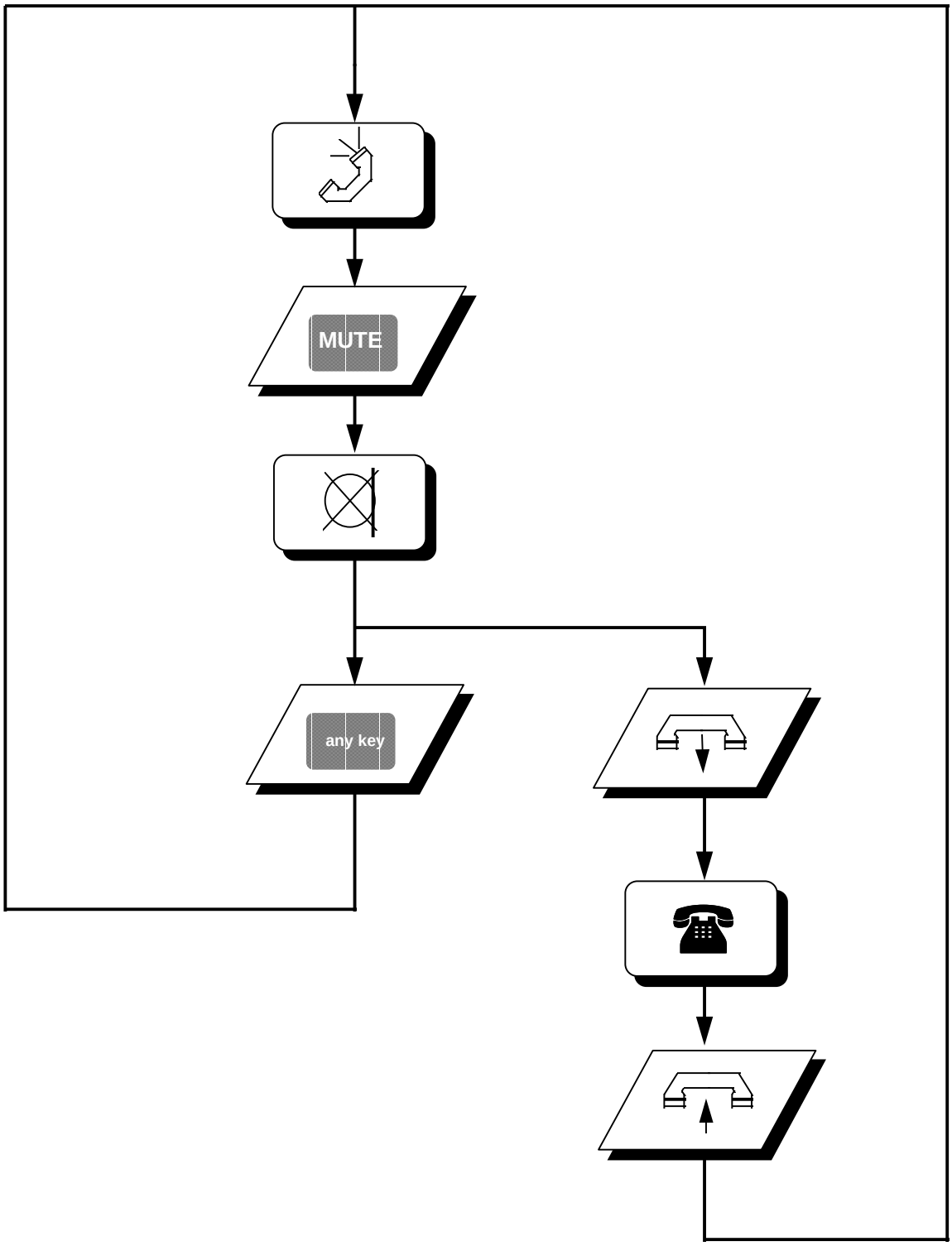
Operating Procedures

The procedures for utilising the features of the SA2532K are optimised out of consideration for the human factor in order to :
- Meet the user's expectations
- be easy to learn

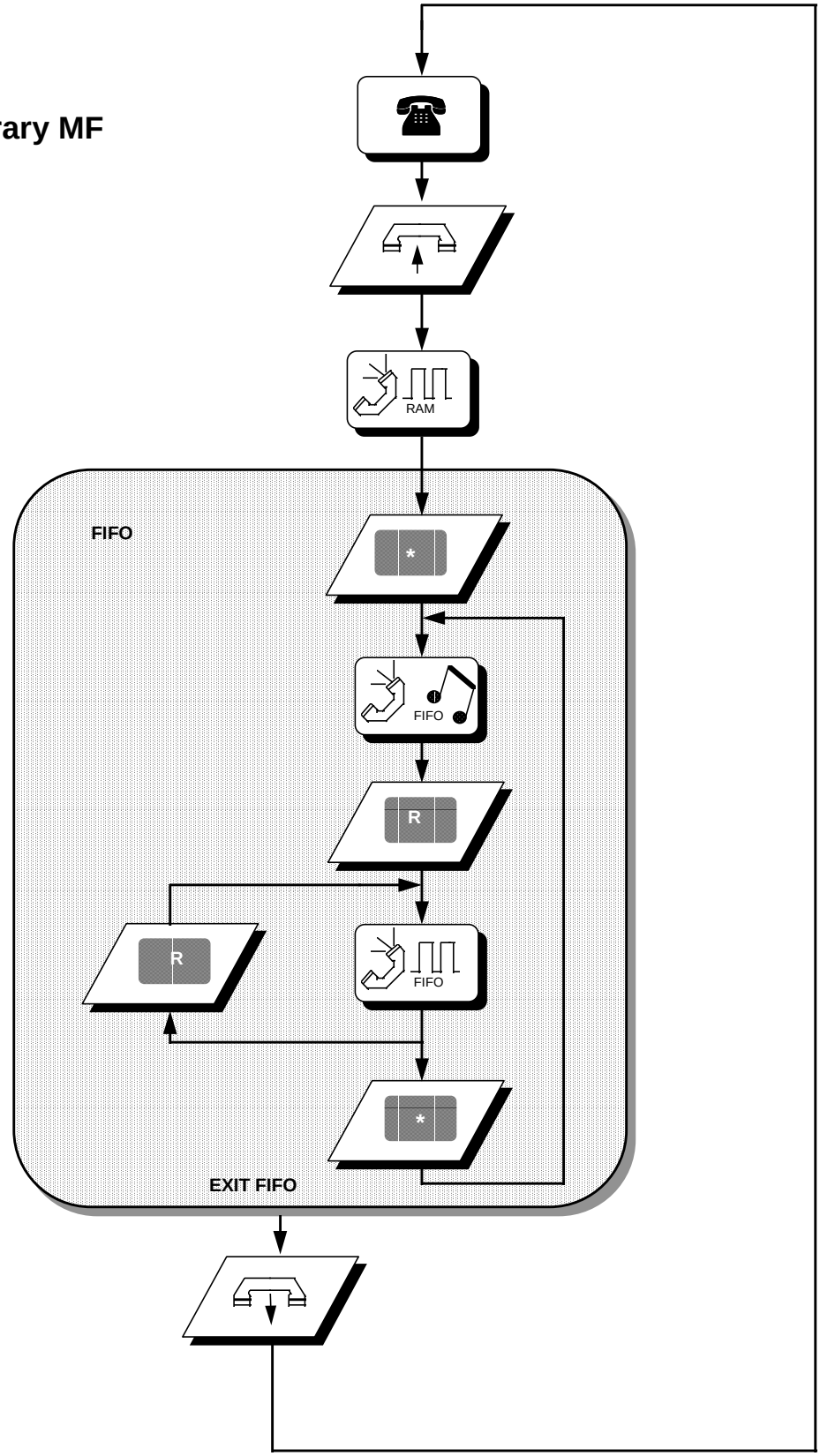
Symbols



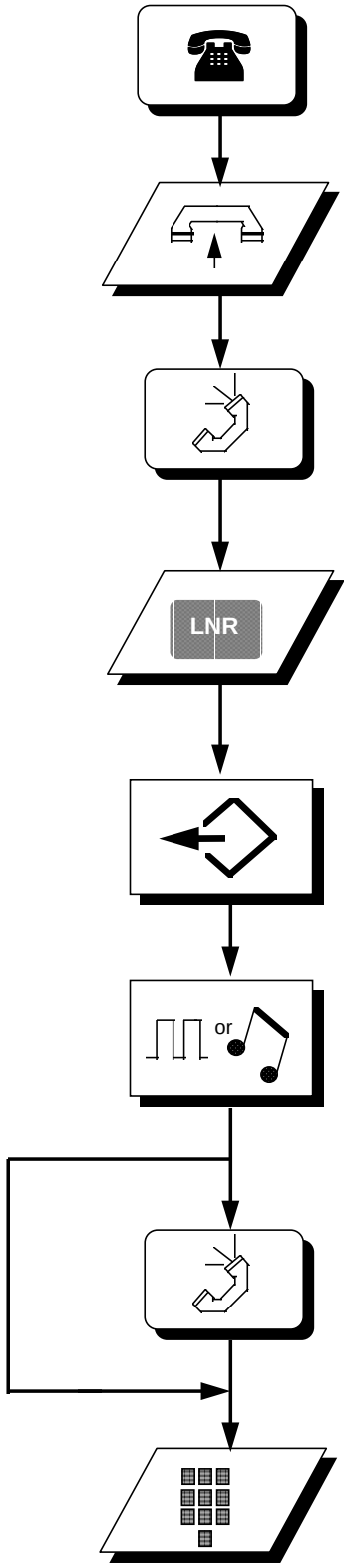
Privacy Mute



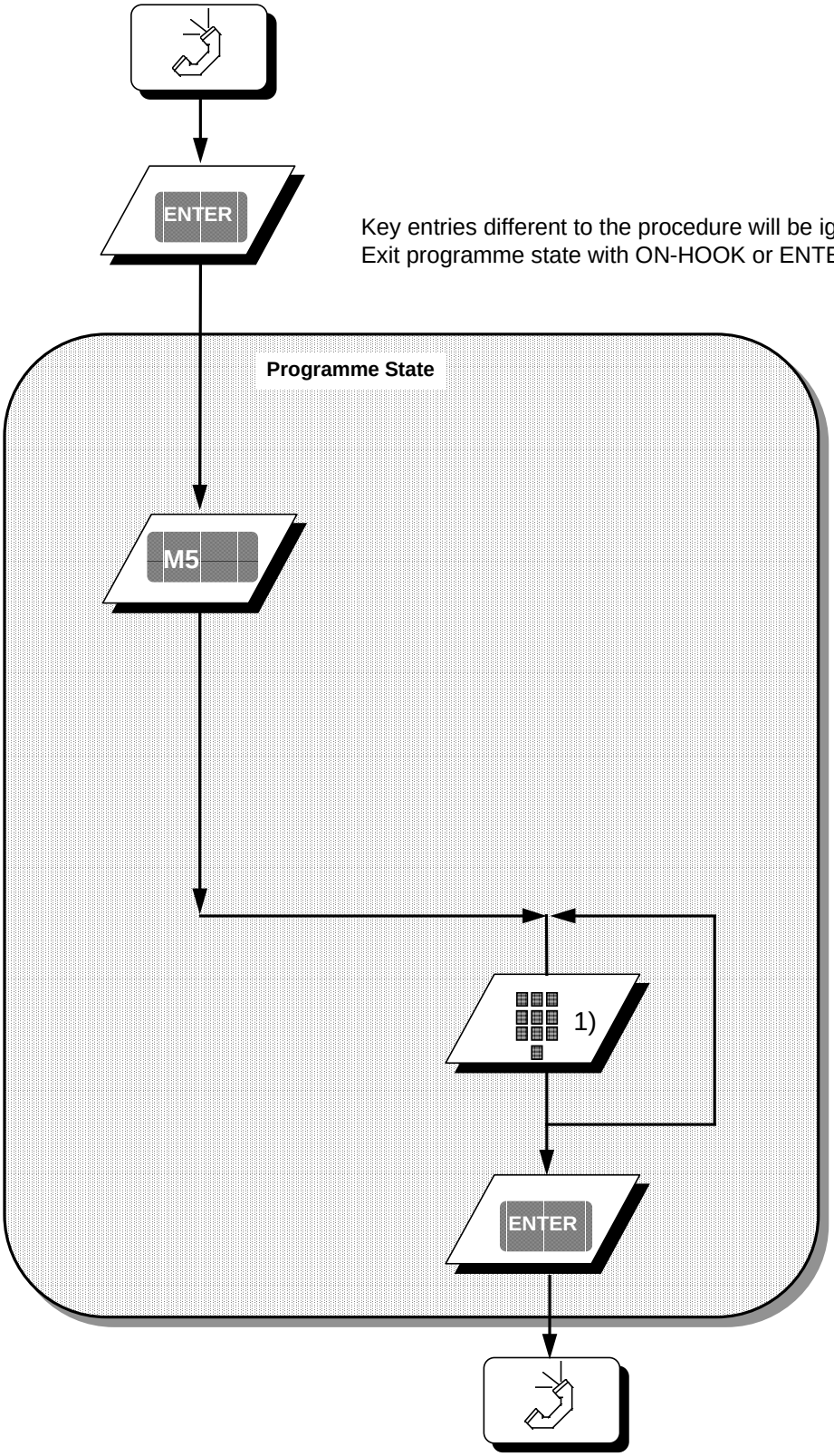
Temporary MF



Last Number Redial (LNR)

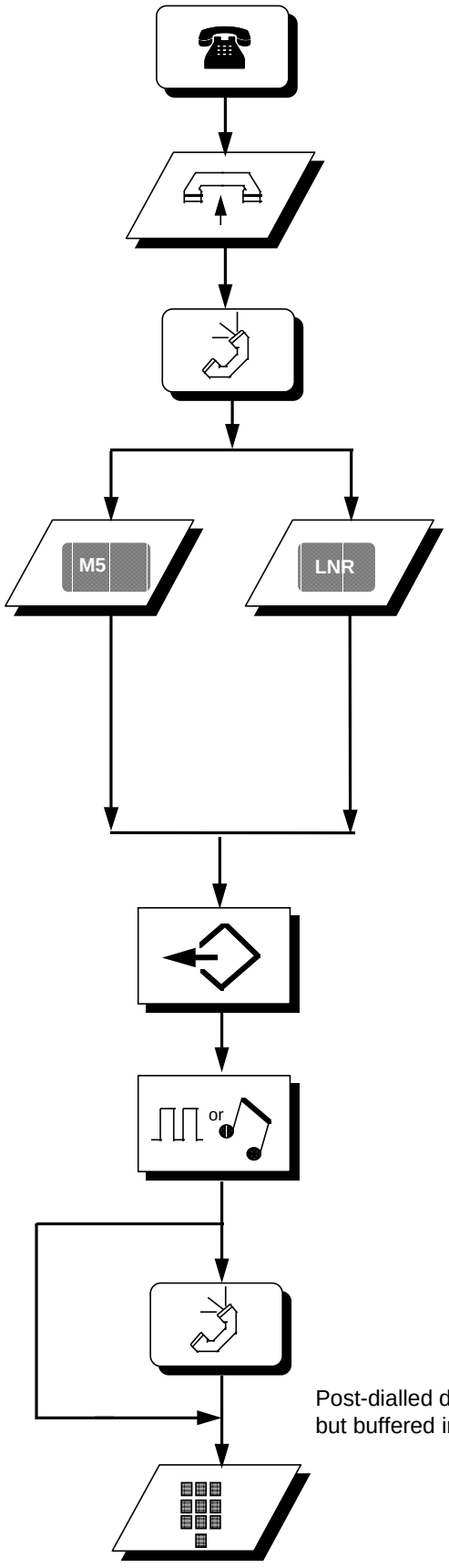


Storing A Number



1) Entries (0-9, *, #, PAUSE, R1, R2) will be stored into the selected memory

Automatic Dialling



Post-dialled digits are not stored
but buffered in FIFO

Electrical Characteristics

Absolute Maximum Ratings

Positive Supply Voltage ..... $-0.3V \leq V_{DD} \leq 7V$
Input current ..... ±25mA
Input Voltage (LS) .... $-0.3V \leq V_{IN} \leq 10V$
Input Voltage (LI, CS) ..... $-0.3V \leq V_{IN} \leq 8V$
Input Voltage (STB, RI) ..... $-2V \leq V_{VIN} \leq V_{DD}+0.3V$
Input Voltage (MO) ..... $-0.3V \leq V_{IN} \leq 35V$
Digital Input Voltage ..... $-0.3 \leq V_{IN} \leq V_{DD}+0.3V$
Electrostatic Discharge ..... ±800V
Storage Temperature ..... -55 ºC to +150ºC

Recommended Operating Conditions

Supply Voltage * (Speech Mode)..... $4V \leq V_{DD} \leq 5V$
Oscillator Frequency (Resonator: Murata CSA 3.58M G300)... 3.58 MHz
Operating Temperature ..... -10ºC to +55ºC

* This voltage is generated internally

DC Characteristics (I_{LINE} = 20 mA unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operating Current	Speech mode MF dialling LD dialling V_{DD} = 2.5V Ring mode V_{DD} = 2.5V		3 4 200 300	5	mA mA uA uA
I_{DDO}	Retention Current	Idle mode V_{DD} = 2V, T_{AMB} = 25ºC		0.05		uA
V_{LI}	Line Voltage (default)	$15mA \leq I_{LINE} \leq 100mA$		4.5		V
I_{OL}	Output Current, Sink CS,HS/DP,MO	V_{OL} = 0.4V		1.5		mA
I_{Oh}	Output Current, Source MODE OUT	$V_{Oh} = V_{DD}$ - 0.4V		-1.5		mA

AC Characteristics (I_{LINE}=20mA; f=800Hz unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TX	**Transmit**	**Test Circuit Fig.5**				
A_{TX}	Gain (M1/M2)	Z_{RI} = 1000 Ω	33.5	35	36.5	dB
$A_{TX/F}$	Variation with Frequency	f=500Hz to 3.4kHz		0.8		dB
THD	Distortion	$V_{LI} \leq 0.5V_{RMS}$			2	%
V_{AGC}	Soft Clip Level	V_{LI} =		2		V_{PEAK}
A_{SCO}	Soft Clip Overdrive			20		dB
t_{ATTACK}	Attack Time			30		us/6dB
t_{DECAY}	Decay Time			20		ms/6dB
Z_{IN}	Input Impedance (M1/M2)			20		kΩ
A_{MUTE}	Mute Attenuation	Mute activated	60			dB
V_{NO}	Noise Output Voltage				-72	dBmp
V_{FC}	Unwanted Frequency Components	50...20 kHZ			-60	dBm
$V_{IN\ MAX}$	Input Voltage Range (M1/M2)	Differential		1		V_{PEAK}
		Single Ended		0.5		V_{PEAK}
BJT	**Output Driver**					
$V_{IN\ MAX}$	Input Voltage Range (LI)			2		V_{PEAK}
V_{TX}	Dynamic Range			2		V_{PEAK}
RL	Return Loss	Z_{RL} = 600 Ohms	15			dB
RX	**Receive**	**Test Circuit Fig.5**				
A_{RX}	Receive Gain (RO1/RO2)	Z_{RL}=600 Ω	0.5	2	3.5	dB
$D_{ARX/F}$	Variation with Frequency	f=500 Hz to 3.4 kHz		0.8		dB
THD	Distortion	$V_{RI} \leq 0.5V_{RMS}$			2	%
V_{AGC}	Soft Clip Level	V_{RI} =		1		V_{PEAK}
A_{SCO}	Soft Clip Overdrive			10		dB
t_{ATTACK}	Attact Time	V_{RI} > 0.8V		30		us/6dB
t_{DECAY}	Decay Time			20		ms/6dB
V_{NO}	Noise Output Voltage				-72	dBmp
V_{FC}	Unwanted Frequency Components	50 Hz...20 kHz			-60	dBm

AC Characteristics (contd) (I_{LINE} = 20mA; f=800Hz unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Z_{IN}	Input Impedance (RI)			8		kΩ
$V_{IN\ RI}$	Input Voltage Range(RI)			2		V_{PEAK}
ST	**Sidetone**	**Test Circuit Fig.5**				
A_{ST}	Sidetone Cancellation	$V_{RI} \leq 0.5\ V_{RMS}$	26			dB
$V_{IN\ ST}$	Input Voltage Range (STB)			2		V_{PEAK}
Z_{IN}	Input Impedance (STB)			80		kΩ
t_D	Keyboard Key Debounce Time			15		ms
	HS Input					
t_{HS_L}	Low to High Debounce	Going off-hook		15		ms
t_{HS_H}	High to Low Debounce	Line breaks/on-hook		240		ms
	DTMF					
ΔF	Frequency deviation	Note 5			1.2	%
V_{MF}	MF Tone Level(Low group)		-9.5	-8	-6.5	dB
V_{L-H}	Preemphasis Low to High		2.0	2.6	3.0	dB
THD	Distortion	Note 3			-30	dBr
t_{TD}	Tone Duration	Note 1	80	82.3	85	ms
t_{ITP}	Inter Tone Pause	Note 1	80	82.3	85	ms
t_{TR}	Tone Rise Time	Note 2			5	ms
t_{TF}	Tone Fall Time	Note 2			5	ms
	LD					
t_{DR}	Dial Rate			10		pps
	tolerance				5	%
$t_{M/R}$	Make/Break	±5%, MODE=low		40/60		ms
	Period	±5%, MODE=high		33/66		ms
t_{PDP}	Pre-Digit Pause			35		ms
t_{IDP}	Inter Digit Pause		750	790	830	ms
t_{MO}	Mute Overhang			156		ms
t_{FD1}	Flash Duration 1		100		102	ms
t_{FD2}	Flash Duration 2		270		276	ms
t_{PFP}	Post Flash Pause			274		ms.

AC Characteristics (contd) (I_{LINE} = 20mA; f=800Hz unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AP}	Access Pause		1.9	2.0	2.1	sec
	Tone Ringer					
V_{MO}	Melody Output Level			PDM		
t_{MD}	Melody Delay				10	ms
F1	Frequency 1		1022	1065	1107	Hz
F2	Frequency 2		1363	1420	1476	Hz
F3	Frequency 3		1664	1734	1803	Hz
t_{DT}	Detection Time	Initial	70		80	ms
t_{TO}	Detection Time-out			Note 4		ms
f_{MIN}	Min. Detection Frequency		12	13	14	Hz
f_{MAX}	Max. Detection Frequency		68	69	70	Hz
	Reminder Tone					
V_{RT}	Level (RO1/RO2)	Relative to LS		-30		dBr
t_{RDT}	Duration			82.3		ms
t_{RTI}	Interval			274		ms
	Comfort Tone (DTMF)					
V_{CT}	Level (RO1/RO2)	Relative to LS		-30		dBr

Note 1: The values are valid during LNR dialling and are minimum values during manual dialling, i.e. the tones will continue as long as the key is depressed.

Note 2: The rise time is the time from 10% of final value until the tone amplitude has reached 90% of its final value.

Note 3: Relative to high group.

Note 4: The FCI circuit is reset by the POR and the HS/DPB pulled high (off hook). After a reset the FCI circuit is in a standby state. A positive edge on FCI will initiate the frequency discrimination. Whenever a period of the ring signal is missing, the timer is reset. When a valid ring signal is present for more than one cycle, the melody generator is started and is directly controlled by the ring signal. This condition will remain until a new reset.

Note 5: This does not include the frequency deviation of the ceramic resonator.

Test Circuit

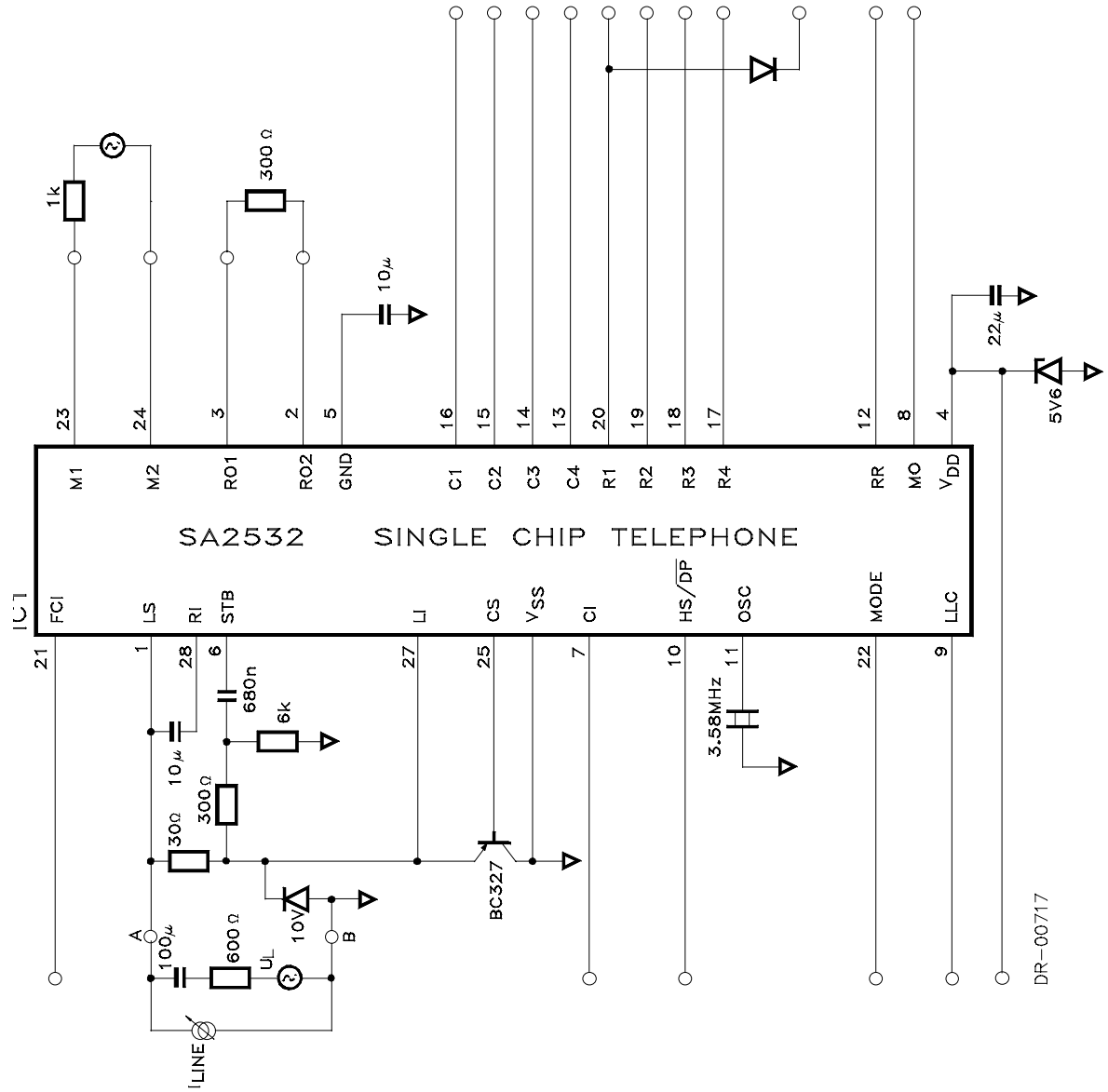


Figure 5

Typical Characteristics of Line Loss Compensation

(f=800Hz, Zline=600Ohm, Vls=-10dBm)

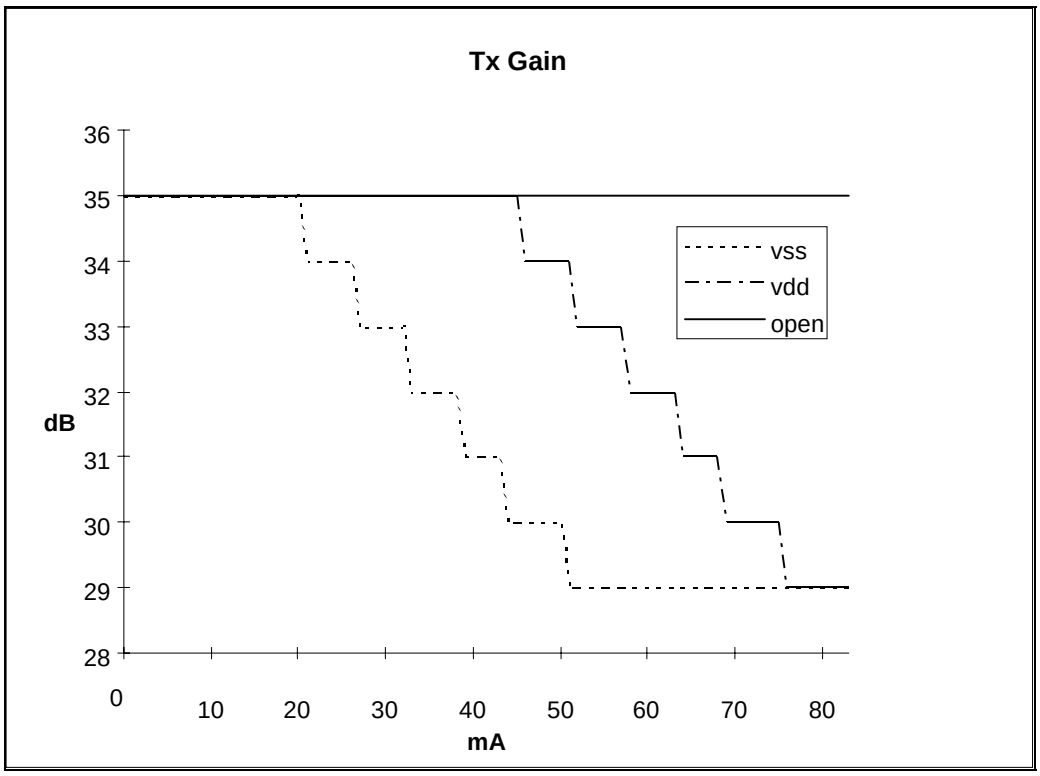


Figure 6

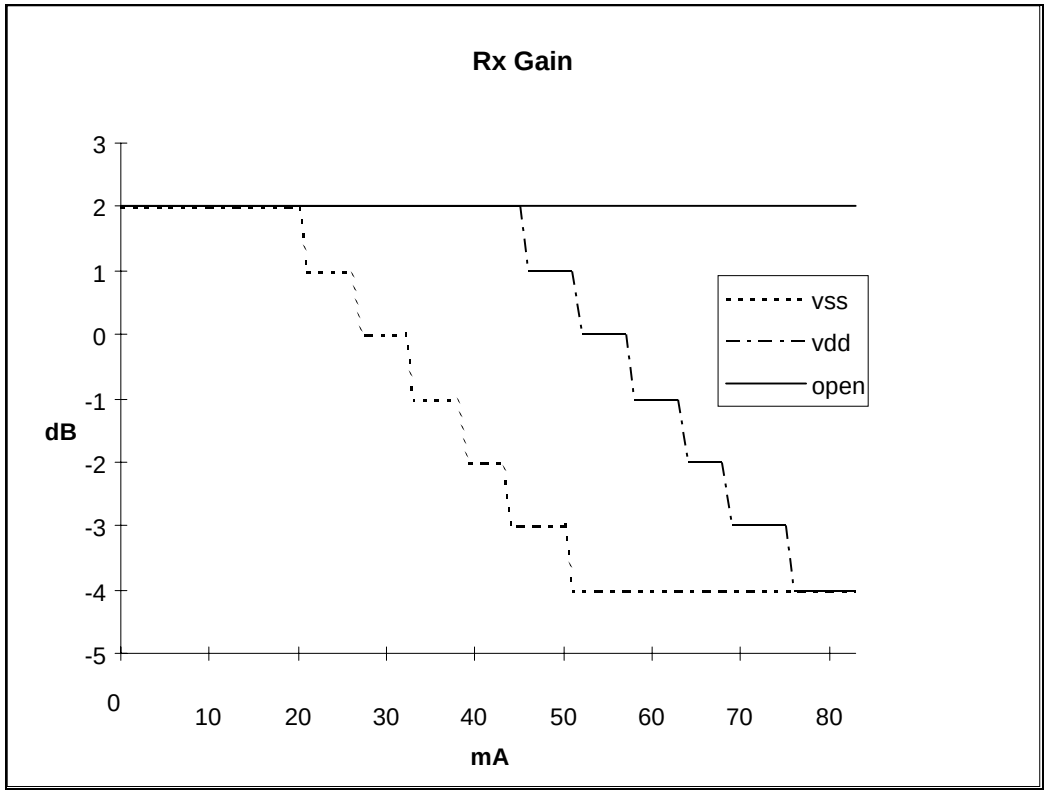


Figure 7

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